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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,288	09/19/2001	Joo-Hyong Lee	LGS/S-0030A	9373

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EXAMINER
DIAZ, JOSE R

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,288	LEE, JOO-HYONG	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 11-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 11-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/290,891* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

➢ Claims 1-4, 13-18, 21-22 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Farrenkopf et al. (US Patent No. 5,899,714).

Regarding claims 1 and 21, Farrenkopf et al. teach a semiconductor device comprising: a semiconductor substrate (20) having a first conductivity type (P-) (see Fig. 2.1 and 2.3); a first well (38D) having a second conductivity type (N-) formed in a first region in a major surface of the semiconductor substrate (see Fig. 2.3); a first MOS transistor (ISO. P-CHAN.) having the first conductivity type (P) and a first contact region (62B) having the second conductivity type (N+) formed in the first well (see Fig. 2.3); and a heavily doped region of buried layer (34D) having the second conductivity type (N+) formed between the first contact region (62B) in the first well (38D) and an interface (24) between the first well (38D) and the semiconductor substrate (20) (see Fig. 2.3).

Regarding claims 2 and 22, Farrenkopf et al. teach a second well (40C) having a second conductivity type (P-) formed in a second region in a major surface of the semiconductor substrate (see Fig. 2.3); a second MOS transistor (ISO. N-CHAN.) having the second conductivity type (N) and a second contact region (60B) having the second conductivity type (P+) formed in the second well (see Fig. 2.3); and a heavily doped region of buried layer (36C) having the first conductivity type (P) formed between the second contact region (60B) in the second well (40C) and an interface (24) between the second well (40C) and the semiconductor substrate (20) (see Fig. 2.3).

Regarding claim 3, Farrenkopf et al. teach that the junction depth of the first and second wells is, for example, in the range of 1.5 to 2.0 μm (see col. 9, lines 13-14 and Fig. 1.1).

Regarding claims 4 and 18, Farrenkopf et al. teach that the concentration of the heavily doped region of buried layer (36C) having the first conductivity type (P) is higher than that of the second well (P-) and lower than that of the second contact region (P+) (see Fig. 2.3).

Regarding claim 13, Farrenkopf et al. further teach a second well (40C) having a first conductivity type (P-) formed in a second region of the semiconductor substrate (20), wherein the heavily doped region of buried layer (34D) having a second conductivity type (N+) is not formed at an interface between the first and second wells (consider the space formed between each heavily doped regions (36C, 34D), wherein a first portion of such a space is located between the heavily doped region 34D and the junction line formed between the wells 40C and 38D, and a second portion of the space

is formed between the heavily doped region 36C and the junction line formed between the wells 40C and 38D. See Fig. 2.3).

Regarding claim 14, Farrenkopf et al. further teach a second well (40C) having a first conductivity type (P-) formed in a second region of the semiconductor substrate (20), and a heavily doped region of buried layer (36C) having a first conductivity type (P) is not formed at an interface between the first and second wells (consider the space formed between each heavily doped regions (36C, 34D), wherein a first portion of such a space is located between the heavily doped region 34D and the junction line formed between the wells 40C and 38D, and a second portion of the space is formed between the heavily doped region 36C and the junction line formed between the wells 40C and 38D. See Fig. 2.3).

Regarding claims 15-16 and 24, Farrenkopf et al. teach a semiconductor substrate (20) having a first conductivity type (P-), a first well (38D) having a second conductivity type (N-) formed in a first region of the semiconductor substrate (20), a second well (40C) having a first conductivity type (P-) formed in a second region of the semiconductor substrate (20), and a heavily doped region of buried layer (34D) having a second conductivity type (N+) not formed at an interface between the first and second wells (consider the space formed between each heavily doped regions (36C, 34D), wherein a first portion of such a space is located between the heavily doped region 34D and the junction line formed between the wells 40C and 38D, and a second portion of the space is formed between the heavily doped region 36C and the junction line formed between the wells 40C and 38D. See Fig. 2.3).

Regarding claims 17 and 25, Farrenkopf et al. further teach a heavily doped region of buried layer (36C) having a first conductivity type (P) not formed at an interface between the first and second wells (consider the space formed between each heavily doped regions (36C, 34D), wherein a first portion of such a space is located between the heavily doped region 34D and the junction line formed between the wells 40C and 38D, and a second portion of the space is formed between the heavily doped region 36C and the junction line formed between the wells 40C and 38D. See Fig. 2.3).

➢ Claims 1-2, 12, 15-16, 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Zunino (US Patent No. 4,646,124).

Regarding claims 1 and 21, Zunino teaches a semiconductor device comprising: a semiconductor substrate (10) having a first conductivity type (P-) (see Fig. 2); a first well (11'a) having a second conductivity type (N-) formed in a first region in a major surface of the semiconductor substrate (see Fig. 2); a first MOS transistor (34) having the first conductivity type (P) and a first contact region (38) having the second conductivity type (N) formed in the first well (see Fig. 2); and a heavily doped region of buried layer (41) having the second conductivity type (N+) formed between the first contact region (38) in the first well (11'a) and an interface (consider the line that separate the epitaxial layer 11 and the substrate 10) between the first well (11'a) and the semiconductor substrate (10) (see Fig. 2).

Regarding claims 2 and 22, Zunino teaches a second well (18b) having a second conductivity type (P) formed in a second region in a major surface of the semiconductor

substrate (see Fig. 2); a second MOS transistor (16) having the second conductivity type (N) and a second contact region (26) having the second conductivity type (P+) formed in the second well (see Fig. 2); and a heavily doped region of buried layer (18a) having the first conductivity type (P+) formed between the second contact region (26) in the second well (18b) and an interface (consider the line that separate the epitaxial layer 11 and the substrate 10) between the second well (18b) and the semiconductor substrate (10) (see Fig. 2).

Regarding claims 12 and 23, Zunino teaches that the heavily doped region (41) of the second conductivity type (N+) does not extend under the first MOS transistor (34) in the first well (11'a).

Regarding claims 15-16 and 24, Zunino teaches a semiconductor substrate (10) having a first conductivity type (P-), a first well (11'a) having a second conductivity type (N-) formed in a first region of the semiconductor substrate (10), a second well (18b) having a first conductivity type (P) formed in a second region of the semiconductor substrate (10), and a heavily doped region of buried layer (41) having a second conductivity type (N+) not formed at an interface between the first and second wells (see Fig. 2).

➢ Claims 1-2, 4-5, and 11-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong (US Patent No. 6,232,165 B1).

Regarding claims 1 and 21, Wong teaches a semiconductor device comprising: a semiconductor substrate (4) having a first conductivity type (P-) (see Fig. 1); a first well

(6) having a second conductivity type (N-) formed in a first region in a major surface of the semiconductor substrate (see Fig. 1); a first MOS transistor (18, 20, 24) having the first conductivity type (P) (see Fig. 1) and a first contact region (consider the heavily doped portion over the region 22) having the second conductivity type (N+) formed in the first well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (22) having the second conductivity type (N+) formed between the first contact region (consider the heavily doped portion over the region 22) in the first well (6) and an interface (consider the junction line at the bottom surface of the first well and adjacent to the substrate) between the first well (6) and the semiconductor substrate (4) (see Figs. 1 and 2G-2H).

Regarding claims 2 and 22, Wong teaches a second well (8) having a second conductivity type (P-) formed in a second region in a major surface of the semiconductor substrate (see Fig. 1); a second MOS transistor (10, 12, 24) having the second conductivity type (N) and a second contact region (consider the heavily doped portion over the region 16) having the second conductivity type (P+) formed in the second well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (16) having the first conductivity type (P) formed between the second contact region (consider the heavily doped portion over the region 16) in the second well (8) and an interface (consider the junction line at the bottom surface of the second well and adjacent to the substrate) between the second well (8) and the semiconductor substrate (4) (see Fig. 1 and 2G-2H).

Regarding claims 4 and 18, Wong teaches that the concentration of the heavily doped region of buried layer (16) having the first conductivity type (**P+**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{12} per cm^2) is higher than that of the second well (**P**) and lower than that of the second contact region (**P++**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{14} per cm^2) (see Figs. 1 and 2G-2H, and col. 4, lines 37-38 and 62-65 and col.5, lines 34-36).

Regarding claims 5 and 19, Wong teaches that the concentration of the heavily doped region of buried layer (22) having the second conductivity type (**N+**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{12} per cm^2) is higher than that of the first well (**N**) and lower than that of the first contact region (**N++**, consider the fact that this region is formed by doping an impurity at a dose of at least 10^{14} per cm^2) (see Figs. 1 and 2G-2H, and col. 4, lines 33-34 and 52-55 and col.5, lines 49-51).

Regarding claims 11 and 20, Wong teaches that the heavily doped region (16) of the first conductivity type (P+) does not extend under the second MOS transistor (10, 12, 24) in the second well (8) (see Figs. 1 and 2G-2H).

Regarding claims 12 and 23, Wong teaches that the heavily doped region (22) of the second conductivity type (N+) does not extend under the first MOS transistor (18, 20, 24) in the first well (6) (see Figs. 1 and 2G-2H).

Regarding claim 13, Wong further teaches a second well (8) having a first conductivity type (P) formed in a second region of the semiconductor substrate (4),

wherein the heavily doped region of buried layer (22) having a second conductivity type (N+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claim 14, Wong further teaches a second well (8) having a first conductivity type (P) formed in a second region of the semiconductor substrate (4), and a heavily doped region of buried layer (16) having a first conductivity type (P+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claims 15-16, Wong teaches a semiconductor substrate (4) having a first conductivity type (P), a first well (6) having a second conductivity type (N) formed in a first region of the semiconductor substrate (4), a second well (8) having a first conductivity type (P) formed in a second region of the semiconductor substrate (4), and a heavily doped region of buried layer (22) having a second conductivity type (N+) not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claim 17, Wong further teaches a heavily doped region of buried layer (16) having a first conductivity type (P+) not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Regarding claims 24-25, Wong teaches a semiconductor device comprising: a semiconductor substrate (4) having a first conductivity type (P-) (see Fig. 1); a first well (6) having a second conductivity type (N-) formed in a first region in a major surface of the semiconductor substrate (see Fig. 1); a first MOS transistor (18, 20, 24) having the first conductivity type (P) (see Fig. 1) and a first contact region (consider the heavily doped portion over the region 22) having the second conductivity type (N+) formed in the first well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (22) having the second conductivity type (N+) formed between the first contact region (consider the heavily doped portion over the region 22) in the first well (6) and an interface (consider the junction line at the bottom surface of the first well and adjacent to the substrate) between the first well (6) and the semiconductor substrate (4) (see Figs. 1 and 2G-2H). Furthermore, Wong teaches a second well (8) having a second conductivity type (P-) formed in a second region in a major surface of the semiconductor substrate (see Fig. 1); a second MOS transistor (10, 12, 24) having the second conductivity type (N) and a second contact region (consider the heavily doped portion over the region 16) having the second conductivity type (P+) formed in the second well (see Figs. 2G-2H and 1); and a heavily doped region of buried layer (16) having the first conductivity type (P) formed between the second contact region (consider the heavily doped portion over the region 16) in the second well (8) and an interface (consider the junction line at the bottom surface of the second well and adjacent to the substrate) between the second well (8) and the semiconductor substrate (4) (see Fig. 1 and 2G-2H). In addition, Wong teaches that the heavily doped region of buried layer (22)

having a second conductivity type (N+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface); and also, that the heavily doped region of buried layer (16) having a first conductivity type (P+) is not formed at an interface between the first and second wells (consider the V-shape formed between the wells 6 and 8, and beneath the region 14-5 in Fig. 1 as the interface). See Fig. 1.

Response to Arguments

➢ Applicant's arguments with respect to claims 1-5 and 11-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Blanchard (US Pat. No. 6,225,662 B1) discloses a buried layer that does not extend under the MOS transistor (see Figs. 5-7).

➢ Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
November 16, 2002

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